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Power- and Low-Resistance-State-Dependent, Bipolar Reset-Switching Transitions in SiN-Based Resistive Random-Access Memory

Sungjun Kim and Byung-Gook Park*

Abstract

A study on the bipolar-resistive switching of an Ni/SiN/Si-based resistive random-access memory (RRAM) device shows that the influences of the reset power and the resistance value of the low-resistance state (LRS) on the reset-switching transitions are strong. For a low LRS with a large conducting path, the sharp reset switching, which requires a high reset power (>7 mW), was observed, whereas for a high LRS with small multiple-conducting paths, the step-by-step reset switching with a low reset power (<7 mW) was observed. The attainment of higher nonlinear current-voltage (I - V) characteristics in terms of the step-by-step reset switching is due to the steep current-increased region of the trap-controlled space charge-limited current (SCLC) model. A multilevel cell (MLC) operation, for which the reset stop voltage (V_{STOP}) is used in the DC sweep mode and an incremental amplitude is used in the pulse mode for the step-by-step reset switching, is demonstrated here. The results of the present study suggest that well-controlled conducting paths in a SiN-based RRAM device, which are not too strong and not too weak, offer considerable potential for the realization of low-power and high-density crossbar-array applications.

Background

Conventional memories such as dynamic random-access memory (DRAM) and NAND flash memory that are based on charge storage have been utilized in many applications until now, and the continually increasing demand for these memories is a response to the era of big data and the Internet of Things (IoT) [1, 2]. In recent years, however, and as expected, a near-future occurrence of the physical limits of these commercial memories has been identified. As an alternative, new approaches such as three-dimensional (3D) structure technology, multilevel cell (MLC) technology, and emerging memory technology have been widely researched [3–5]. Among the emerging memories, the resistive random-access memory (RRAM) has attracted considerable interest due to numerous advantages that include a simple structure, a fast switching speed, a low-voltage operation, an extendibility to the 3D

structure, and an MLC operation [6–31]. Although extensive research has been carried out on the oxide-based RRAM that is a strong candidate for nonvolatile memory applications, it is also worth investigating a nitride-based RRAM with a silicon bottom electrode (BE), as it has a complete compatibility with the standard complementary metal-oxide-semiconductor (CMOS) processing [26–31]. So far, however, only a small amount of discussion regarding the resistive-switching characteristics of the nitride-based RRAM has occurred.

In particular, MLC is an important key technology for high-density nonvolatile memories and synaptic devices, as it overcomes the limits of conventional lithography [32]. In the RRAM, the MLC can be easily achieved through a controlling of the stop voltage (V_{STOP}) for reset switching. The main aim of this study is a clarification of the switching parameters to differentiate the three types of reset-switching transition in terms of a fabricated Ni/Si₃N₄/p⁺-Si-based RRAM device.

* Correspondence: bgpark@snu.ac.kr

Department of Electrical and Computer Engineering, Inter-University Semiconductor Research Center (ISRC), Seoul National University, Seoul 08826, South Korea

Methods

The sample was prepared as follows: After the standard cleaning processes, a p^+ Si BE was highly doped using a BF_2^+ ion implanting with a dose of $5 \times 10^{15} \text{ cm}^{-2}$ (converted to a peak concentration of 10^{20} cm^{-3}). A SiN layer of 4.1 nm thickness was then deposited on the implanted silicon wafer using low-pressure chemical vapor deposition (LPCVD) at 785°C after an annealing process was performed at 1050°C for 10 min; subsequently, the Ni top electrode (TE) was deposited and patterned through a shadow mask that contains circular patterns with a $100\text{-}\mu\text{m}$ radii. All of the electrical properties were characterized at room temperature according to the DC voltage sweep mode and the pulse mode using the Keithley 4200-SCS semiconductor parameter analyzer (SPA) and the 4225-PMU ultra-fast I - V module, respectively. Also, the p^+ -Si BE was grounded and control biases were applied to the Ni TE over the measurements.

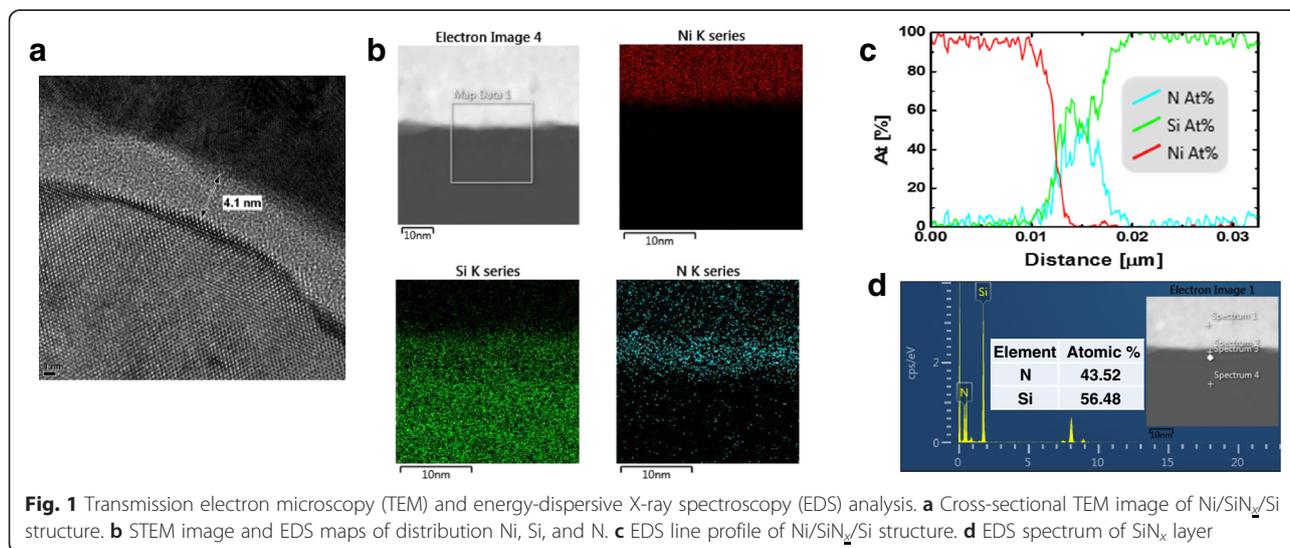
Results and Discussion

The thickness of SiN_x layer was confirmed using cross-sectional transmission electron microscopy (TEM) image of Ni/SiN_x/Si structure as shown in Fig. 1a. Scanning TEM (STEM) image and energy-dispersive X-ray spectroscopy (EDS) maps of distribution Ni, Si, and N is shown in Fig. 1b. Atomic percentage of each layer was confirmed by EDS line profile and spectrum of Ni/SiN_x/Si structure as shown in Fig. 1c, d, respectively.

Figure 2a shows the bipolar current-voltage (I - V) characteristics of the Ni/Si₃N₄/ p^+ -Si RRAM device under the DC voltage sweep mode. After the positive electroforming process (a thick black line), a current compliance (CC) of 5 mA was used to activate a pristine cell with a high initial resistance; here, the CC is used to protect the device from a permanent dielectric breakdown. A

negative voltage sweep was conducted without the CC for the reset process that performs a switch from the low-resistance state (LRS) to the high-resistance state (HRS). A positive sweep switches the device back to the LRS for the reset switching. The Ni/Si₃N₄/ p^+ -Si RRAM device then showed a forming-less process, indicating that the forming voltage is within the distribution range of the set voltage; notably, with the 5-mA CC, sharp current drops were observed for all of the reset switching during 100 consecutive DC voltage sweeps. Alternatively, the set switching, whereby the current is increased sharply or gradually, is more complicated; also, for some of the switching, the set process was completed after a gradual current drop due to an incomplete reset switching, suggesting that the set and the reset switching are strongly affected by the previous switching events.

Next, the reset-switching behaviors under a $100\text{-}\mu\text{A}$ CC were investigated. According to the I - V characteristics that are shown in Fig. 2b–d, reset switching can be classified into three types. Figure 2b shows a sharp reset switching that occurs even though a low CC of $100 \mu\text{A}$ was set for the device. The low LRS resistance and high reset current (I_{RESET}) are caused by a current overshoot that is for the set process. The main reason for the occurrence of the current overshoot is an instrument-response time that is slower than the switching time of the device. Figure 2c exhibits a step-by-step reset transition that starts with a relatively high LRS resistance; here, the comparability of the I_{RESET} to the CC of $100 \mu\text{A}$ is probably due to a reduced overshoot effect that occurs during the set process. Figure 2d shows a weak reset switching, where the current drop is within only a few microamperes and the LRS resistance is very slightly changed; here, it is likely that the weakness is due to an incomplete formation of the conducting path



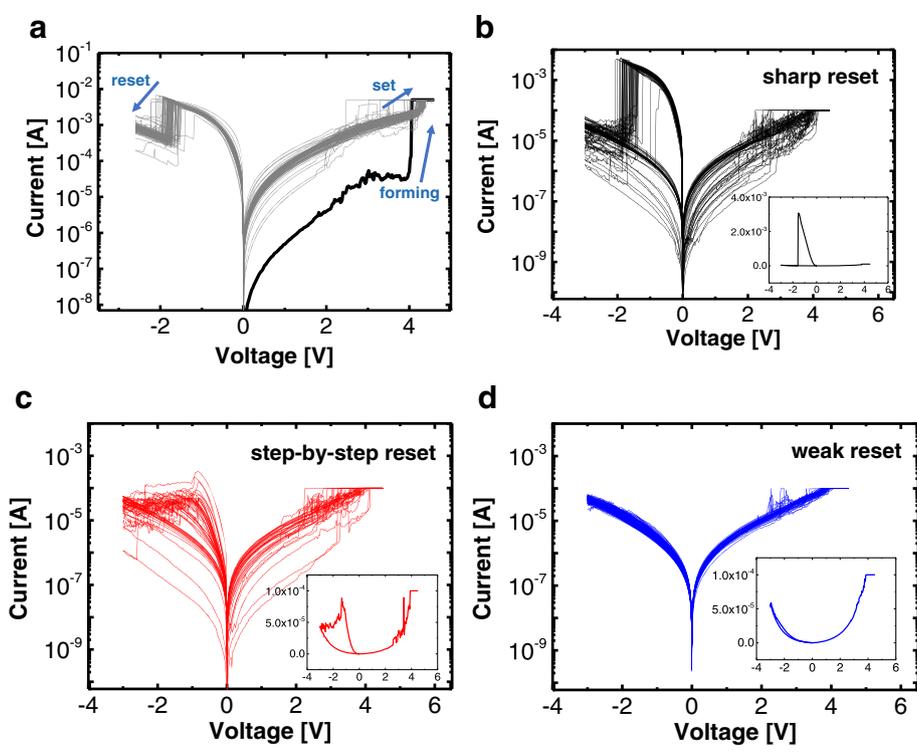


Fig. 2 *I-V* characteristics of the Ni/Si₃N₄/p⁺-Si RRAM device. **a** Sharp reset transition with CC of 5 mA. **b** Sharp reset transition with CC of 100 μA. **c** Step-by-step-reset transition with CC of 100 μA. **d** Weak reset transition with CC of 100 μA

in terms of the set process. The current overshoot effect in the proposed fabricated device occurs randomly, and this causes a large variation of the LRS [33, 34]. If appropriate actions such as a series resistance and a transistor were prepared for the device to reduce the current overshoot, the CC could control the LRS resistance and the reset current more efficiently [35, 36]; however, the provision of a clue to gain an understanding of the reset-transition behaviors in the LRS itself is worthwhile. Figure 3 shows the cumulative frequency of the LRS and HRS resistances for the three types of reset switching. The distribution of the sharp reset switching is less dispersive compared with the distribution of the step-by-step reset switching. For the weak reset switching, only a slight difference is evident between the LRS and the HRS. According to the findings of this paper, a proper set overshoot is needed to obtain an effective resistive-switching behavior.

Through the double logarithmic plots of the *I-V* curve in the LRS, a preliminary estimation of the conducting mechanism of the fabricated device was made. The current transport is governed by a power law (i.e., $I \sim V^m$), but with different slopes, as shown in Fig. 4. The ohmic behavior ($I \sim V$) was changed to Child's square law ($I \sim V^2$) for the three types of switching, and a higher slope region ($I \sim V^m$, $m > 2$) was observed for the switchings with

the step-by-step and the weak reset transitions. This conduction can be explained by the trap-controlled space charge limited current (SCLC) theory [37–41]. The trap sites that are composed of the dangling bonds in the trivalent Si atoms can be used as a medium through the trapping and de-trapping of the carriers. The ohmic conduction in a low-voltage region is dominated by free electrons that are thermally dominated

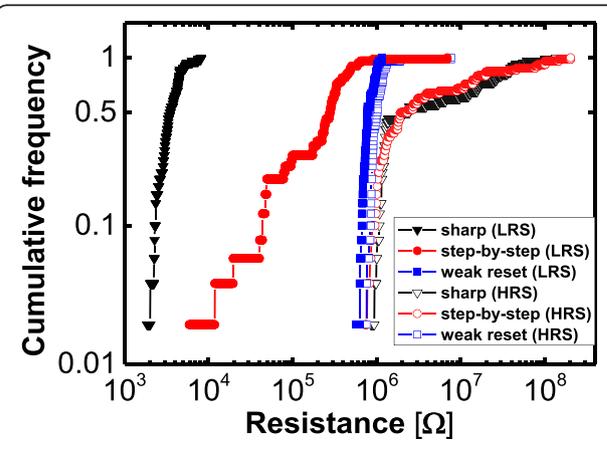
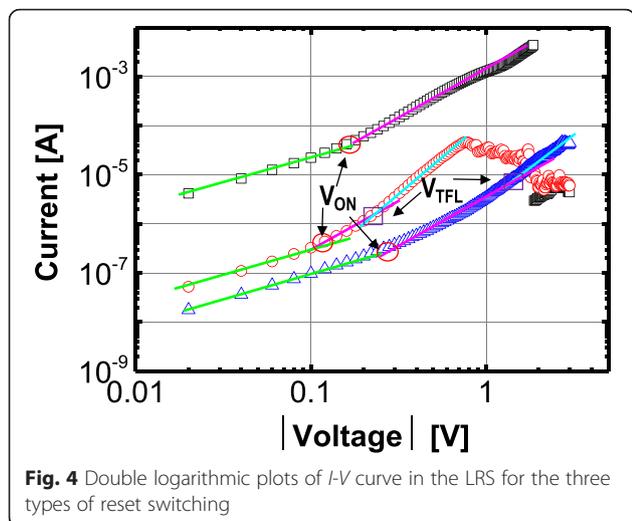


Fig. 3 Cumulative frequency of the LRS and HRS resistances for the three types of reset switching



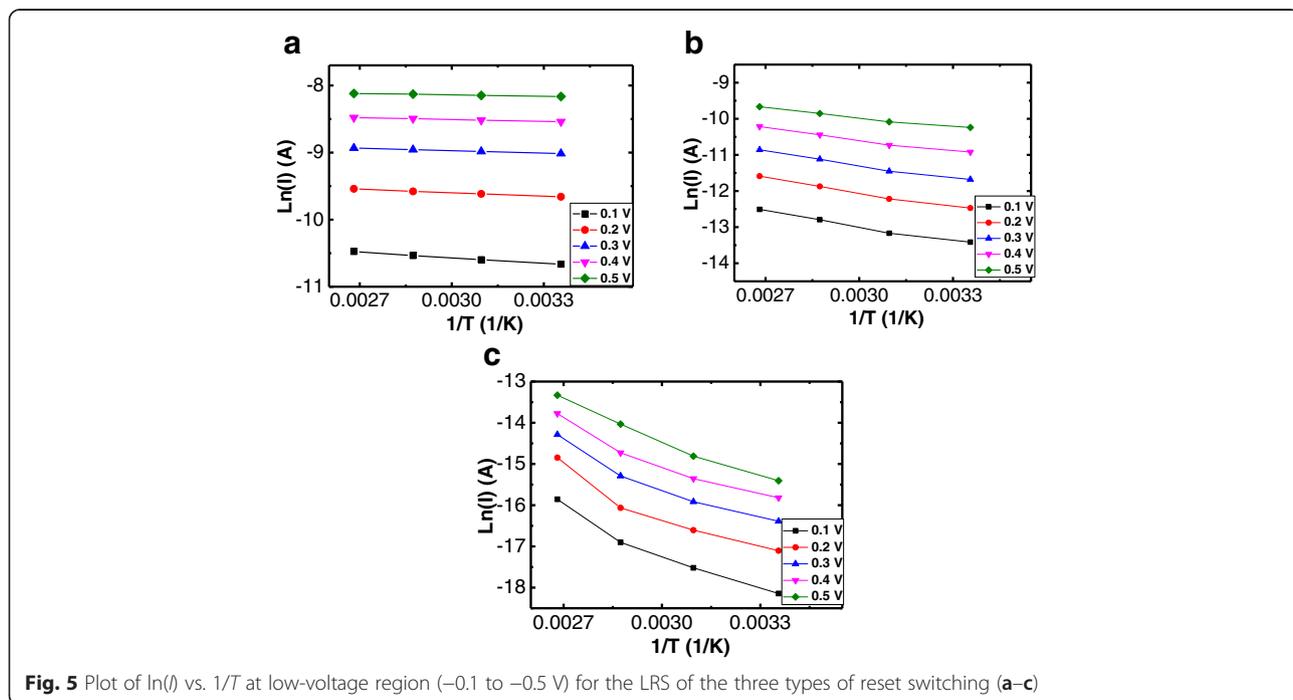
when they are compared to the injected electrons. The injected electrons from the electrode become especially predominant with the increasing of the voltage at the V_{ON} that can be expressed as follows:

$$V_{ON} = [8/9(\theta + \theta_t)/\theta] \cdot [qn_0L^2/\epsilon_r\epsilon_0],$$

where θ is the free carrier density, θ_t is the concentration of the traps, q is the electron charge, n_0 is the thermally produced free-electron density, L is the nitride thickness, ϵ_r is the static-dielectric constant, and ϵ_0 is the permittivity of the free space. The trap-unfilled SCLC is

changed to a trap-filled SCLC at the trap-filled limited voltage (V_{TFL}), thereby resulting in a further slope increase. The sharp reset switching was finished before the V_{TFL} was reached, while the switchings with the step-by-step reset and the weak reset were completed after the V_{TFL} was reached.

Unlike the conventional metal-oxide-based RRAM devices such as NiO, TiO₂, and CuO₂, for which a metallic ohmic conduction with a slope of 1 in the log-log scale is shown, SiN_x-based RRAM devices exhibited nonlinear I - V curves in the LRS. The nonlinear resistive switching in the LRS is one of the major strong points in the two-terminal-based crosspoint array application. The earlier report for which the Ni/SiN/TiN RRAM stack is used confirmed this intrinsic nonlinear characteristic, which is attributed to the different trap-assisted tunneling mechanism that applies in this case; here, the nonohmic I - V curves of the Ni/SiN/ p^+ -Si RRAM device can also be explained by the different properties of the conducting path in the LRS. The metallic conducting paths of the metal-oxide-based RRAM that are in the LRS are formed by oxygen vacancies. In this case, the resistance is increased when the temperature is elevated; contrarily, the SiN-based RRAM employs the previously mentioned trap-related conduction mechanism that ensures the production of a nonlinear I - V curve without the use of an extra selection device. Figure 5a–c shows the plot of the $\ln(I)$ vs. the $1/T$ in the low-voltage region (-0.1 to -0.5 V) for the LRS of the three types of reset switching. A negative slope indicates that the underlying conduction mechanism is based on a trap-to-trap hopping that



occurs through nitride vacancies, rather than the intervention of the metallic conducting filaments. Figure 6 shows the nonlinearity of the three types of reset switching in the LRS. The selectivity can be defined as the ratio of the current at the read voltage (V_{READ}) to that at half of the V_{READ} ($1/2 V_{\text{READ}}$). The selectivity of the step-by-step reset switching is higher than that of the sharp reset switching by more than the absolute value of 0.4 V, and this is because the steep increased current in the high-voltage region after the V_{TFL} of 0.5 V is reached leads to a higher nonlinearity for the step-by-step reset switching.

As part of the authors' determination of the reset-transition behaviors, a further investigation of the switching parameters was conducted, whereby the relationship between the resistive-switching parameters was closely examined. Figure 7a shows the I_{RESET} as a function of the LRS resistance in terms of the switchings with the sharp and the step-by-step resets. The sharp-reset-switching relationship between the two parameters is not clear; alternatively, for the switching with the step-by-step reset, the I_{RESET} is decreased with an increasing of the LRS resistance. Notably, the three reset types are determined by the LRS resistance in the inset of Fig. 7a, indicating that, for the step-by-step reset switching, the conducting paths are carefully controlled for the set switching. Figure 7b shows the scatter plot of the I_{RESET} vs. V_{RESET} in terms of the switchings with the sharp and the step-by-step resets. The I_{RESET} is directly proportional to the absolute V_{RESET} value for the sharp and the step-by-step resets; meanwhile, the step-by-step reset shows the opposite trend. The inset of Fig. 7b shows the distribution of the reset power (P_{RESET}) of the switchings with respect to both the sharp and the step-by-step resets. The two reset transitions are clearly distinguished by an I_{RESET} of 7 mA and a P_{RESET} of 1 mW.

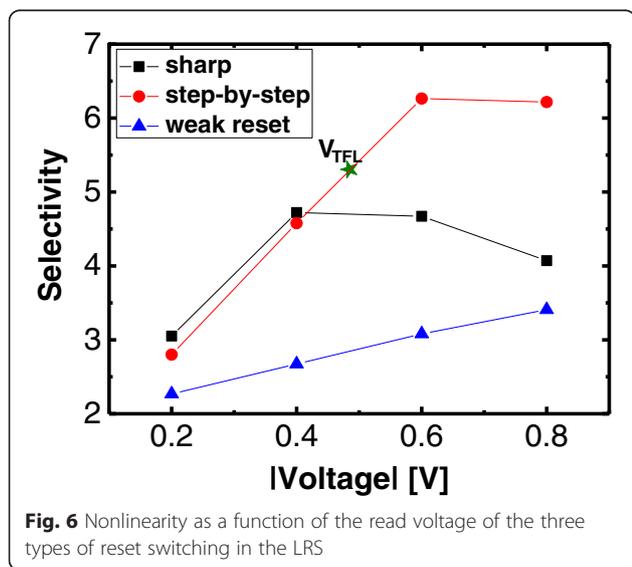


Fig. 6 Nonlinearity as a function of the read voltage of the three types of reset switching in the LRS

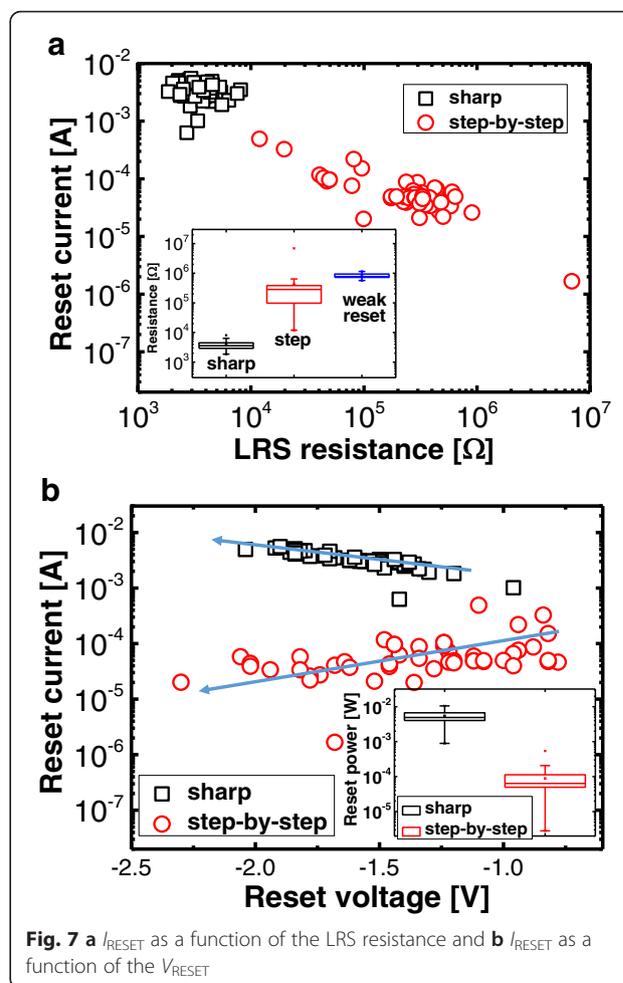


Fig. 7 a I_{RESET} as a function of the LRS resistance and b I_{RESET} as a function of the V_{RESET}

To evaluate the MLC capability, the DC characteristics of the Ni/SiN/ p^+ -Si device were investigated through a controlling of the V_{STOP} . Figure 8a shows the multilevel I - V characteristics of the reset process for the step-by-step reset switching. The current levels of the multiple states were gradually decreased by more than three orders of magnitude, while the V_{STOP} was increased from -1.3 to -2.5 V; moreover, the pulse characteristics were checked for the three switching types. Figure 8b shows the resistance value after the different pulse amplitudes from -2 to -5 V were applied to the devices; for the abrupt reset switching, a switching response was not registered until -4.5 V and a sharp current drop was observed at -5 V. For the step-by-step reset switching, an initially higher LRS resistance is required for the employment of the MLC operation; however, a weak resistance change was obtained for the initially very high LRS resistance that is caused by the set switching. It is therefore important to ensure a proper LRS resistance range after the set switching for the MLC operation. Figure 8c, d shows the applied voltage pulse (-3 and -5 V) and the

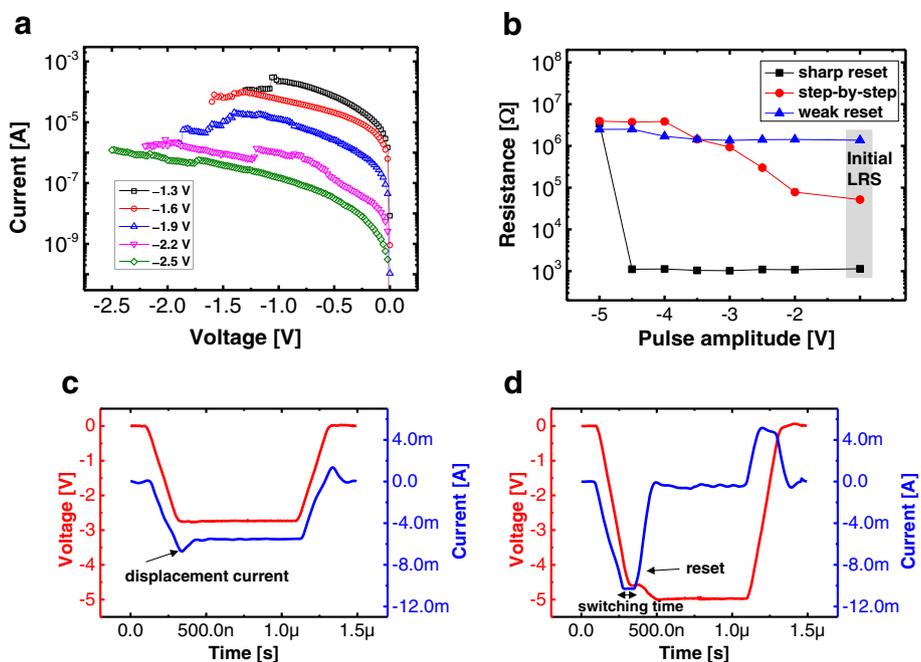


Fig. 8 **a** Multilevel I - V characteristics of the reset process for step-by-step reset switching. **b** Resistance value after different pulse amplitudes from -2 to -5 V are applied to the devices. Applied voltage pulse (-3 **c** and -5 V **d**) and transient current response for sharp reset switching

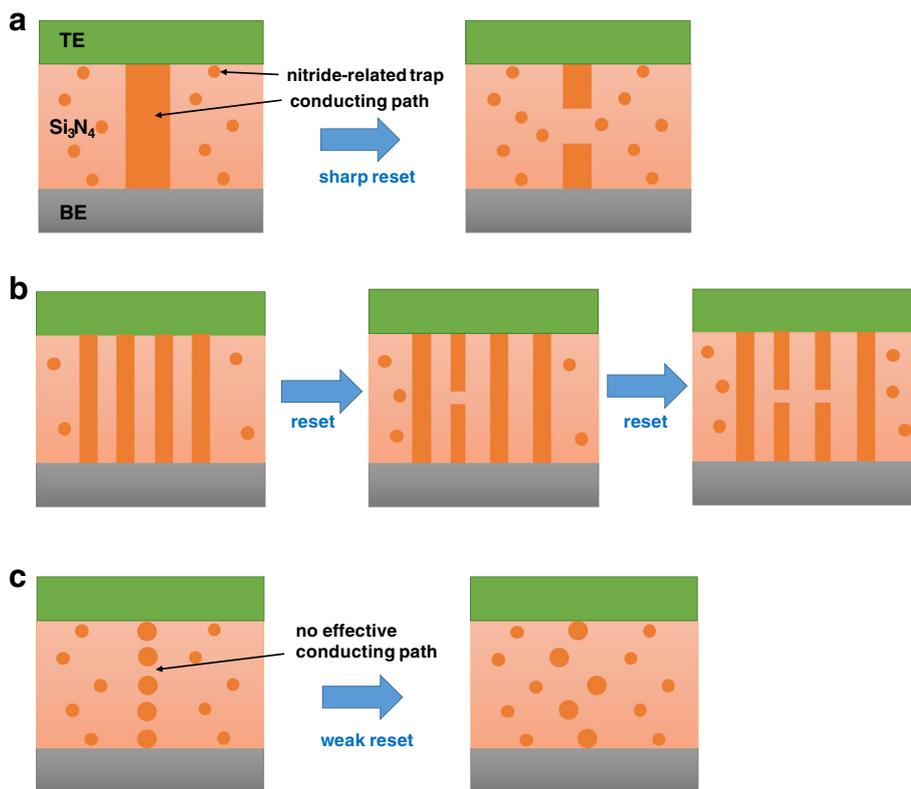


Fig. 9 Schematics showing possible reset-switching models for the three types of reset-switching behavior: **a** sharp reset, **b** step-by-step reset, and **c** weak reset

transient current response for the sharp reset switching. A significant current change was not recorded during the peak voltage of -3 V after the occurrence of an external displacement current, which is caused by the capacitive charging effect in the test system that is shown in Fig. 8c; alternatively, a distinctive current drop was observed when the peak voltage of -5 V was applied to the device.

Based on the electrical measurement results, a possible reset-switching model is proposed in this paper for the three types of reset-switching behavior, as shown in Fig. 9a–c. The conducting path may be made up of abundant traps which originate from dangling bonds in the trivalent Si atoms. Here, we explain the switching and conduction mechanism for three reset switching transitions by using conduction path model. Three reset-switching transitions can be explained by the size of conducting paths, which is related to the amount of traps [42]. For the sharp reset switching, however, a singly connected large conducting path could be ruptured; that is, the sharp reset process that is caused by the electrical field with thermal assistance turns to the HRS, as shown in Fig. 9a. For the step-by-step reset switching, the weakest part among the multiple conducting paths would be ruptured first, followed by the additional rupture processes, as shown in Fig. 9b. For a weak reset switching, initially weak conducting paths would be formed, followed by the absence of an effective reset process, as shown in Fig. 9c.

Conclusions

The different bipolar reset transitions in terms of an Ni/SiN/Si RRAM device were investigated in this study depending on the reset power and the resistance value of the LRS, which is determined by the forming and set processes. The sharp reset switching was observed for the high reset power (>7 mW) and the low LRS, whereas the step-by-step reset switching was observed for the low reset power (<7 mW) and the high LRS. Higher nonlinear I - V characteristics and a gradual reset change regarding the step-by-step reset switching would be two of the most virtuous merits of the low-power and high-density crossbar array.

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Authors' contributions

SK prepared the samples and electrical measurements and wrote the manuscript. BGP provided technical support to the study. Both authors read and approved the final manuscript.

Competing interests

The authors declare that they have no competing interests.

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